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PATENT
Serial No. 09/730,679
Amendment in Reply to Office Action of 12-28-05

IN THE CLAIMS

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JAN 24 2006

Please amend claims as follows:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) A synchronization method suitable for a system comprising at least a station of a first type and a station of a second type, both of which include a transmitting part having a transmit timing controller for capable of transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with capable of synchronizing data transmitted from stations to provide a receive timing, characterized in that it the method comprises the following steps:

- providing the receiving part of the station of the second type with a synchronization circuit that generates chip fractions shifted in time,
- measuring a receive clock deviation made at the stations of the second type, and
- adjusting a transmit clock at the station of the second type by adopting the opposite deviation value to compensate for a frequency shift due to a movement of the station of the second type.

6. (Cancelled)

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7. (Cancelled)

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8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Previously Presented) A method as claimed in Claim 5, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

17. (Previously Presented) A method as claimed in Claim 16, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output that contains chip fraction previously produced at the first output.

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18. (Previously Presented) A method as claimed in Claim 17, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

19. (Previously Presented) A method as claimed in Claim 18, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

20. (Previously Presented) A method as claimed in Claim 19, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.

21. (Cancelled)

22. (Cancelled)

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